AMENDMENTS TO THE CLAIMS

This Listing of the Claims will replace all prior versions, and listings, of claims in this application.

Listing of the Claims:

1. (Currently Amended) A communications device for detecting user transmitted symbols encoded in spread spectrum waveforms (hereinafter "user waveforms") comprising

a digital signal processor (hereinafter "DSP") that processes user waveforms to determine characteristics thereof, the DSP having an associated memory and an associated direct memory access (hereinafter "DMA") controller that controls access to that memory, and

a programmable logic device (hereinafter "PLD") that is coupled to the DMA controller and that configures it to move data relating to user waveform characteristics from the memory to a buffer external to the DSP,

wherein said user waveform characteristics comprise one or more waveform amplitudes.

2. (Original) The device of claim 1, wherein the PLD configures the DMA controller to move the data from the memory to the buffer in blocks.

3. (Original) The device of claim 2, wherein the PLD configures the DMA controller to move the data from the memory to the buffer in unfragmented blocks.

4. (Original) The device of claim 2, wherein the PLD configures the DMA controller to move the data from the memory to the buffer in fragmented blocks.

5. (Original) The device of claim 4, wherein the PLD formats the fragmented blocks in the buffer for subsequent defragmentation.

6. (Currently Amended) A communications device for detecting user transmitted symbols encoded in spread spectrum waveforms (hereinafter " user waveforms") comprising

a first-in first-out buffer comprising a dual-port random access memory,

a digital signal processor (hereinafter "DSP") that processes user waveforms to determine characteristics thereof, the DSP having an associated memory and an associated direct access memory (hereinafter "DMA") controller that controls access to that memory,

a programmable logic device (hereinafter "PLD") that is coupled to the DMA controller and that configures it to move data relating to user waveform characteristics from the memory to the buffer external to the DSP,

wherein said user waveform characteristics comprise one or more waveform amplitudes.

7. (Original) The device of claim 6, wherein the programmable logic device is any of a field programmable gate array and a applications specific integrated circuit.

8. (Currently Amended) The device of ~~according to~~ claim 6, comprising a multi-port data switch coupled with the PLD.

9. (New) The device of claim 1, wherein said waveform characteristics further comprise amplitude ratios of said user waveforms.